LOW-K ISOLATION SPACERS FOR CONDUCTIVE REGIONS

1) FIELD OF THE INVENTION

[0001] The invention is in the file of Semiconductor Structures.

2) DESCRIPTION OF RELATED ART

[0002] For the past several years, the miniaturization and higher packing density of conductive regions in semiconductor structures, such as gate electrodes or metal interconnects, has been accompanied with an increase in fringe capacitance. Fringe capacitance, i.e. "cross-talk," between such conductive regions may be detrimental to the performance of, for example, semiconductor devices or interconnect networks.

[0003] In order to overcome any dominant effects of fringe capacitance, higher power input may be provided to the semiconductor structure. However, this approach has drawbacks for today's low power requirements, e.g. extending battery life. Thus, a methods to isolate conductive regions in semiconductor structures is described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. **1** illustrates a cross-sectional view representing a conductive region isolation by a pair of two-component low-k isolation spacers, in accordance with an embodiment of the present invention.

[0005] FIG. **2**A-K illustrates cross-sectional views representing the formation of a planar MOS-FET with a gate electrode isolated by a pair of two-component low-k isolation spacers, in accordance with an embodiment of the present invention.

[0006] FIG. **3** illustrates a cross-sectional view representing a planar MOS-FET with a gate electrode isolated by a pair of two-component low-k isolation spacers, wherein the source/drain regions are faceted, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0007] A process for fabricating semiconductor structures and the resultant structures are described. In the following description, numerous specific details are set forth, such as specific dimensions and chemical regimes, in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known processing steps, such as patterning steps or wet chemical cleans, are not described in detail in order to not unnecessarily obscure the present invention. Furthermore, it is understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0008] Disclosed herein is a multi-component (two or more components) low-k isolation spacer for isolating conductive regions in a semiconductor structure and a method to form a pair of two-component low-k isolation spacers for a gate electrode in a semiconductor device. Multi-component low-k isolation spacers comprised of higher-k upper portions robust to processing conditions and protected lower-k lower portions may enable a reduction in fringe capacitance and, hence, may enable low power operation of conductive regions. Thus, in accordance with an embodiment of the present invention, a multi-component spacer is used to isolate a conductive region in a semiconductor structure, enabling operation of the semiconductor structure with a reduced power consumption.

[0009] Isolation spacers may be used to physically separate neighboring conductive regions in a semiconductor structure, while protecting each of the conductive regions during various processing steps. A multi-component low-k isolation spacer may provide the same physical separation and protection of the conductive region as a conventional single-component isolation spacer, but may also enable a reduction in fringe capacitance, i.e. "cross-talk," between conductive regions within a semiconductor structure. In accordance with an embodiment of the present invention, a multi-component low-k isolation spacer is formed directly adjacent to the sidewall of a conductive region. At least a portion of the multi-component isolation spacer is comprised of a low-k material and, therefore, fringe capacitance may be reduced significantly.

[0010] In addition to providing protection to and isolation for a conductive region, an isolation spacer should be sufficiently robust to withstand typical processing steps, such as ion bombardment implant steps, wet chemical cleans steps and dry etch steps (e.g. contact formation). Often, a higher-k material is required to provide such a robust isolation spacer, while a lower-k material is usually detrimentally impacted by such processing steps. Thus, in keeping with the requirement of robustness, in accordance with an embodiment of the present invention, at least a portion of the multi-component isolation spacer is comprised of a higher-k material, e.g. a material with a dielectric constant of at least 4.0. In a specific embodiment, the upper portion of the multi-component low-k isolation spacer is comprised of a higher-k material that provides durability and robustness to inhibit degradation of the multi-component low-k isolation spacer during processing steps. Meanwhile, the lower (protected) portion of the multi-component low-k isolation spacer is comprised of a lower-k material that enables a reduced fringe capacitance.

[0011] A replacement isolation spacer technique may be used to incorporate a multi-component low-k isolation spacer into a semiconductor structure with a conductive region. For example in accordance with an embodiment of the present invention, a replacement isolation spacer processing scheme is used to form a two-component isolation spacer wherein the top portion of the two-component isolation spacer is comprised of a higher-k material that provides durability and robustness, while the bottom portion is comprised of a lower-k material that enables a reduced fringe capacitance. Thus, the more fragile, lower-k portion is protected by the more robust higher-k portion.

[0012] In a metal-oxide-semiconductor field-effect transistor (MOS-FET), the incorporation of a raised source/drain region can increase the fringe capacitance between the raised source/drain region and a nearby gate electrode. Thus, in accordance with an embodiment of the present invention, a multi-component low-k isolation spacer is formed directly between a raised source/drain region and a gate electrode via a replacement isolation spacer processing scheme. The multi-component low-k isolation spacer physically separates (and hinders electrical shortage between) the raised source/drain region and the gate electrode, while mitigating fringe capacitance.